METHOD OF FORMING METALLIC LAYER UTILIZING ATOMIC LAYER VAPOR DEPOSITION METHOD AND SEMICONDUCTOR ELEMENT USING THE SAME

METHOD OF FORMING METALLIC LAYER UTILIZING ATOMIC LAYER VAPOR DEPOSITION METHOD AND SEMICONDUCTOR ELEMENT USING THE SAME

Patent Number:

JP2001217206

Publication date: 2001-08-10

Inventor(s):

KYO SHOHAN;; RIN GENSHAKU;; CHAE YUN-SOOK;; ZEN RINSO;; SAI

KICHIGEN

Applicant(s):

SAMSUNG ELECTRONICS CO LTD

Requested

Patent:

JP2001217206

Application

Number:

JP20000371636 20001206

Priority Number(s):

C23C16/34; H01L21/285;

C23C16/44: H01L21/203; H01L27/04;

Classification:

H01L21/822; H01L27/105; H01L27/108; H01L21/8242

EC

Classification:

FC

Classification:

Equivalents:

TW444278

Abstract

PROBLEM TO BE SOLVED: To provide a metallic layer forming method by which superior step coverage can be obtained by utilizing an atomic layer vapor deposition method, a desired resistance and electrical conductivity can be decided easily, and then, the diffusion of oxygen can be prevented, and to provide a semiconductor element equipped with a metallic layer formed by the method as a barrier metal layer or the lower or upper electrode of a capacitor. SOLUTION: In this metallic layer forming method, atomic layers are alternately laminated upon another by alternately injecting source gases of a reactive metal A, nitrogen N, and an element B for amorphous coupling of the metal A with nitrogen N into a chamber by the atomic layer vapor deposition method. The semiconductor element is provided with a metallic layer formed by this method as a barrier metal layer, lower electrode, or upper electrode.